REMARKS

The following remarks are submitted to be fully responsive to the non-final Office Action of September 24, 2007. Claims 28-29, 33, 35, and 37-39 are pending in the present application. Reconsideration in view of the following remarks is respectfully requested.

First, Applicants wish to thank Primary Examiner Wells for conducting the personal interview with Applicants' undersigned attorney on January 7, 2008. Although no agreement was reached, Applicants' undersigned attorney noted that the use of a "substantial current," as taught in col. 1, lines 53-61 of Baskett (USP 6,333,672), teaches away from "trickle currents [that] are approximately 10 to 100 times smaller than said first current," as recited in independent claim 28. Accordingly, even if Baskett were combined with Applicants' Prior Art FIG. 1, the noted feature or the advantages thereof would not be met, as substantially discussed during the interview, as set forth in detail below.

Independent claim 1 is patentably distinguishable over Baskett and Applicants' Prior Art FIG. 1, alone or in combination, because Baskett and Applicants' Prior Art FIG. 1, alone or in combination, fail to disclose, teach or suggest all of the features recited in the pending claims. For example, independent claim 28 (emphasis added) recites:

> A digital to analog converter comprising:
> a first analog current summing bus having one end coupled to ground;
> a second analog current summing bus having one end coupled to ground; and
> a plurality of current switches, each switch including:
> **a first current source for supplying a first current**;
> a differential pair of transistors adapted to couple said first current to either the first current summing bus or the second current summing bus in response to a pair of complementary input signals;
> a pair of cascode transistors having emitters respectively coupled to the collectors of said differential pair of transistors, and collectors coupled to the other ends said first and second current summing buses, respectively; and
> **second and third current sources adapted to respectively supply first and second trickle currents** to the emitters of said pair of cascode transistors in order to maintain said pair of cascode transistors in an `on' state regardless of the states of said differential pair of transistors,
> **wherein the trickle currents are approximately 10 to 100 times smaller than said first current.**

Thus, independent claim 28 is directed to a novel digital to analog converter having a first current source for supplying a first current, and second and third current sources adapted to respectively supply first and second trickle currents, wherein the trickle currents are approximately 10 to 100 times smaller than the first current. Advantageously, with Applicants' invention of independent claim 28, the trickle currents are set as small as possible, so as to reduce power (see, e.g., ¶¶ [0008], and [0026] of Applicants' published Specification), but also high enough to allow the cascode transistors to settle (see, e.g., ¶¶ [0027], [0031], and [0032] of Applicant's published Specification), and contrary to the teaching away therefrom by Baskett col. 1, lines 53-61.

By contrast, Baskett and Applicants' Prior Art FIG. 1, alone or in combination, do not disclose, teach or suggest the novel digital to analog converter having a first current source for supplying a first current, and second and third current sources adapted to respectively supply first and second trickle currents, wherein the trickle currents are approximately 10 to 100 times smaller than the first current, as recited in independent claim 28 and claims dependent therefrom, nor the advantages thereof. Specifically, the present Office Action correctly notes that Applicants' Prior Art FIG. 1 does not include a pair of cascode transistors, and second and third current sources adapted to respectively supply first and second trickle currents to emitters of the pair of cascode transistors.

The present Office Action attempts to cure the noted deficiencies in Applicants' Prior Art FIG. 1 by relying on cascode amplifiers 12 and 14 and respective keep alive current sources 16 and 18 of Prior Art FIG. 1 of Baskett. However, even if Baskett's cascode amplifiers 12 and 14 and respective keep alive current sources 16 and 18 were combined with Applicants' Prior Art FIG. 1, the noted feature or advantages of the invention of independent claim 28 would not be met. Specifically, Baskett at col. 1, line 41 to col. 2, line 3 discloses (emphasis added) that:

> Referring to FIG. 1, an improved prior art differential logic circuit 10 is illustrated which provides one method of reducing switching delays induced by toggling the conduction states of differential input transistor pairs by using cascode amplifiers. Transistors 12 and 14 provide a cascode amplifier arrangement such that the voltage variation at nodes 26 and 28 is reduced. Reducing voltage variation at nodes 26 and 28 reduces the miller capacitance effect seen at terminals D and D-compliment, which reduces switching delays through prior art differential logic circuit 10. Voltage variation at nodes 26 and 28 can be further reduced by the addition of keep

> alive current sources 16 and 18. Keep alive current sources 16 and 18 provide a nominal amount of current flowing through cascode amplifiers 12 and 14 regardless of the conduction state of transistors 20 and 22, respectively. **Sizing the keep alive current sources 16 and 18 such that current conduction through transistors 16 and 18 is a substantial portion of the total current entering nodes 26 and 28, respectively, the corresponding voltage variation at nodes 26 and 28 can be significantly reduced, thus substantially eliminating the miller effect**. As logic families develop, however, the required input logic voltage swings diminish which inherently diminishes the magnitude of the miller effect. Additionally, as logic families develop, the top supply rail potential diminishes which requires reducing the number of base-emitter voltage (V.sub.be) drops between top and bottom supply rail potentials. New logic families, therefore, no longer have the top supply rail potential headroom to support a cascode amplifier configuration to reduce the miller effect.

By contrast, the invention of independent claim 28 requires that the trickle currents (e.g., I_{T2} and I_{T3} of FIG. 3) are approximately **10 to 100 times smaller** than the first current (e.g., I_1 of FIG. 3) and which Baskett teaches away from by requiring current conduction through the keep alive current sources 16 and 18 to be a **substantial** portion of the total current entering nodes 26 and 28.

In addition, setting the trickle currents to be approximately 10 to 100 times smaller than the first current is not a mere design choice, but rather provides the noted and other advantages discussed throughout Applicants' Specification. Accordingly, one of ordinary skill in the art at the time of the invention of independent claim 28 would find no motivation to modify the combination of Baskett and Applicants' Prior Art FIG. 1 to set the trickle currents to be approximately 10 to 100 times smaller than the first current, in view of Baskett's teaching away therefrom, and absent improper hindsight reconstruction of Applicants' invention based on Applicants' disclosure.

Therefore, independent claim 28 is allowable over Baskett and Applicants' Prior Art FIG. 1, alone or in combination. The dependent claims 29, 33, 35, and 37-39 are allowable over Baskett and Applicants' Prior Art FIG. 1, alone or in combination, on their own merits, and for at least the reasons advanced above with respect to independent claim 28.

In view of the foregoing, it is submitted that the present application is in condition for allowance and a notice to that effect is respectfully requested. However, if the Examiner deems that any issue remains after considering this response, the Examiner is invited to contact the undersigned attorney to expedite the prosecution and engage in a joint effort to work out a mutually satisfactory solution.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 50-2478 and please credit any excess fees to such deposit account.

Respectfully submitted,

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